Agilent Technologies

PCI Express™ Logic Analyzer Probing Design Guide for Agilent Technologies

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Agilent Technologies

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1.1 Objectives

This document is intended to provide Agilent Technologies customers with insight into the information needed by platform and system design teams for integration of Logic Analyzer Probing for PCI Express™ into their designs. In its complete form, this information provides system designers a mechanical and electrical solution space for Logic Analyzer Interface (LAI) placement for the PCI Express bus. The solutions given here only concern a mid-bus probing solution in which the LAI footprint is designed into the target system. Agilent will also plans to provide a low intrusion interposer/extender to support slot connectors on the PCI Express™ bus.

Although information concerning PCI Express™ topology and specifications will be given, this document is not intended to take the place of other PCI Express design documentation. **It is assumed that a design team utilizing this document for their design constraints will validate their designs through pre and post route electrical simulation and keepout volume analysis.** To enable proper consideration to the numerous design parameters, a layout/schematic checklist has been developed and is included as an appendix in this document.

1.2 Nomenclature

- LAI refers to the Analysis Probe or Agilent N4220A
- Midbus Connection, midbus probe, Midbus LAI and Midbus footprint refer the LAI Footprint Connector or the Agilent N4221A PCI Express™ Compression Cable set. ½ Midbus Connection, ½ midbus probe, ½ Midbus LAI and 8 Channel PCI Express* LAI Pinout midbus footprint refer the LAI Footprint Connector or the Agilent N4228A PCI Express™ Compression Cable set.

2 Overview and Configuration Support

2.1 Link Configuration Support

A PCI Express™ LAI provides support for a 16 channel mid-bus direct probing solution. For the purposes of this document, “channel” refers to either an upstream differential pair OR downstream differential pair for a given lane. A corollary statement is that “channel” refers to either a transmit differential pair OR receive differential pair for a given lane. Flexibility is given to the platform designer to configure a probing solution that best meets the needs of the system. With this 16 channel solution, the following configurations may be made¤:

- Upstream and downstream channels of one x8 link
- Upstream and downstream channels of up to two x4, x2, or x1 links
- Upstream or downstream channels of one x16 link
- Upstream or downstream channels of up to four x8, x4, x2, or x1 links
- Other combinations may be available. Contact Agilent Technologies for the latest support configurations

¤As long as the LAI placement within the system requirements are met (see section 4.1.1 - LAI Placement within System Topology). System designers should verify that their system requirements are supported by the LA vendors by contacting Agilent Technologies* directly.

2.2 Reference Clock(s) To LAI

Each system must provide means of delivering a reference clock (for each PCI Express™ reference clock domain) for specific cases:

- When an LAI is used with a system that supports Spread Spectrum Clocking (SSC) on the reference clock to all the PCI Express™ agents and the SSC can not be disabled
- When testing must be done with SSC enabled because a problem does not manifest with SSC disabled
- If the link frequency is intentionally margin tested outside the standard +/-300ppm tolerance.

- If any clock domain reference clock operates outside a +/-150ppm tolerance (note that this is more restrictive than the PCI Express™ standard of +/-300ppm, but must be considered). For more information, contact contacting Agilent Technologies directly.

Note that this clock can be a dedicated clock, in which case appropriate terminators must be provided on the board. Alternately, the signals may be a tap off an existing clock, since the probes are designed to not significantly load the signals. However, this needs to be verified by the system platform designers to verify proper functionality. See Reference Clock Model (Fig. 10) for more information.

3 Mechanical Design

This section contains mechanical design details (footprint dimensions, keepout volumes, and part numbers) of the midbus LAI and the reference clock pin header.

3.1 Midbus LAI

3.1.1 N4221A - Footprint Dimensions and Specifications

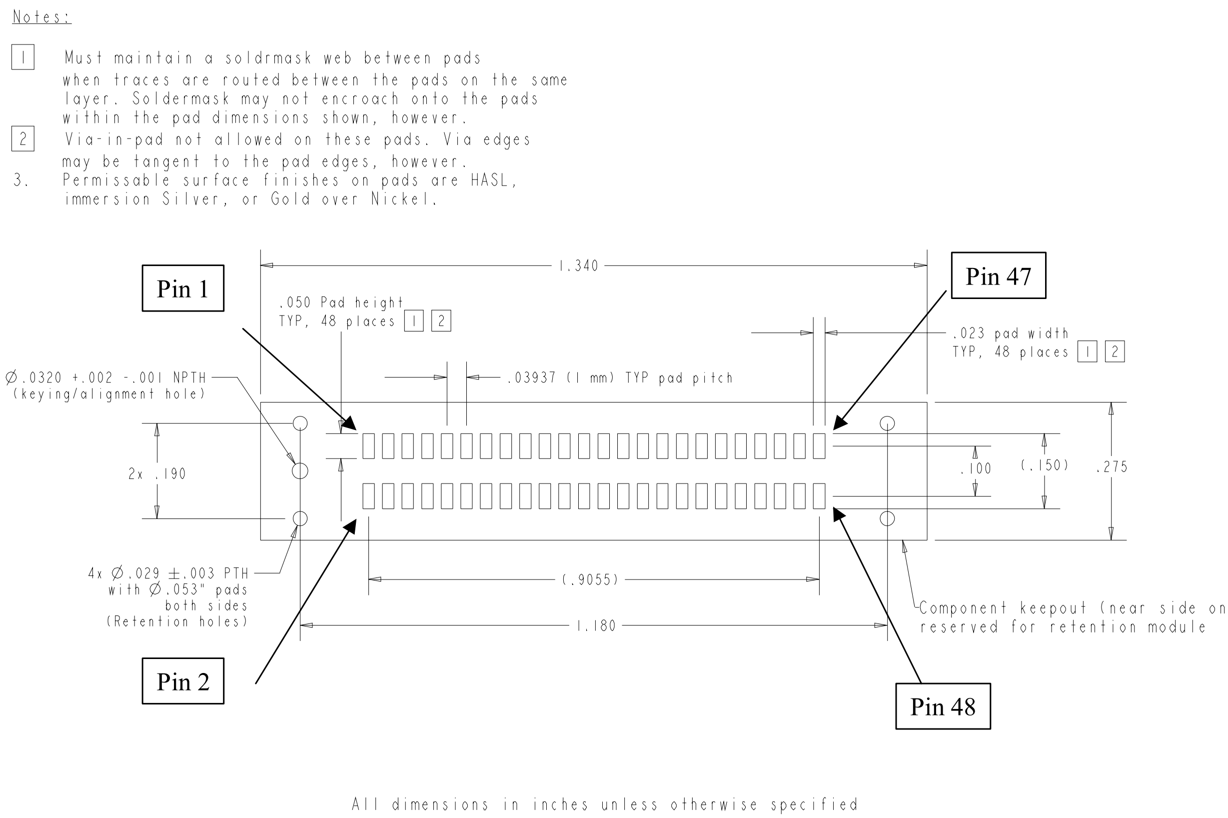
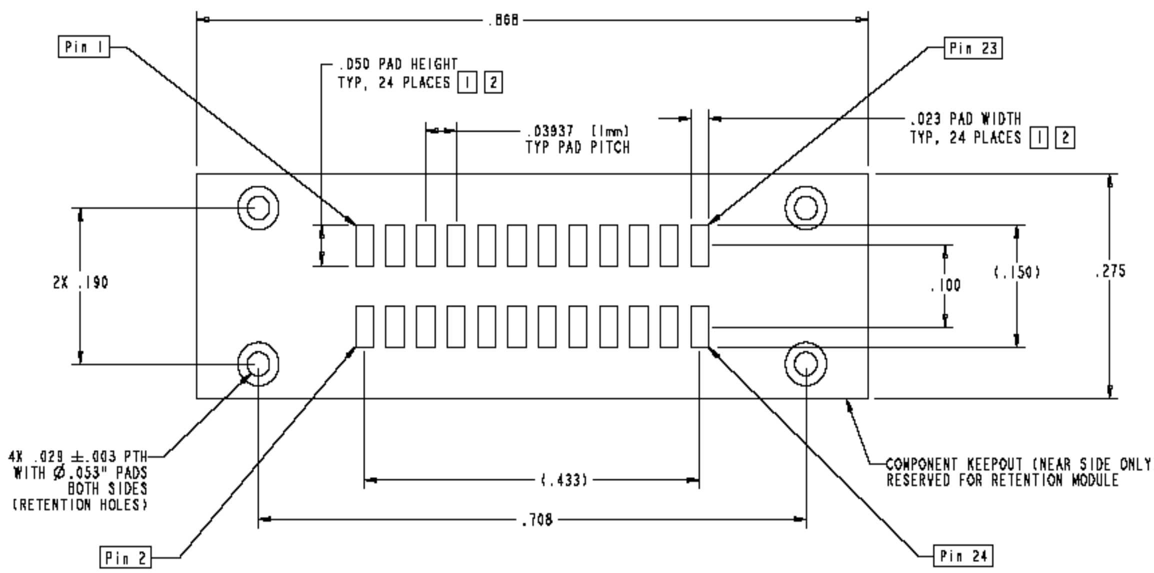


Figure 1- PCI Express™ LAI footprint dimensions, pin numbering, and specification

3.1.2 N4228A – ½ Size midbus Footprint Dimensions and Specifications

NOTES:

1. MUST MAINTAIN A SOLDERMASK WEB BETWEEN PADS WHEN TRACES ARE ROUTED BETWEEN THE PADS ON THE SAME LAYER. HOWEVER, SOLDERMASK MAY NOT ENCROACH ONTO THE PADS WITHIN THE PAD DIMENSIONS SHOWN.
2. VIA-IN-PAD NOT ALLOWED ON THESE PADS. HOWEVER, VIA EDGES MAY BE TANGENT TO THE PAD EDGES.
3. PERMISSABLE SURFACE FINISHES ON PADS ARE HASL, IMMERSION SILVER, OR GOLD OVER NICKEL.



ALL DIMS IN INCHES UNLESS OTHERWISE SPECIFIED

3.1.3 N4221A - Keepout Volume

Keepout volume for the PCI Express™ LAI is given in Figure 2. For more specific information on keepout volumes for particular solutions contact Agilent.

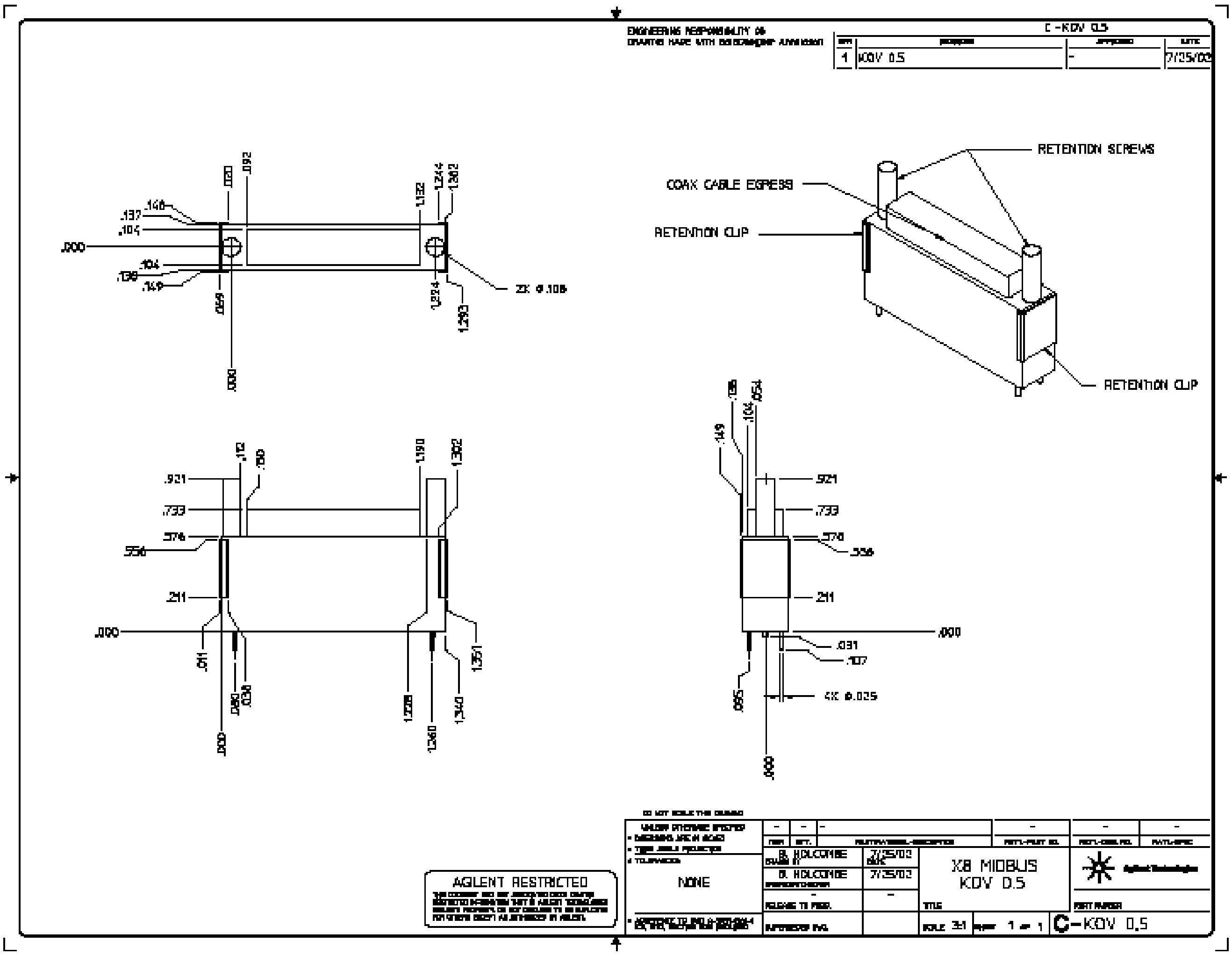
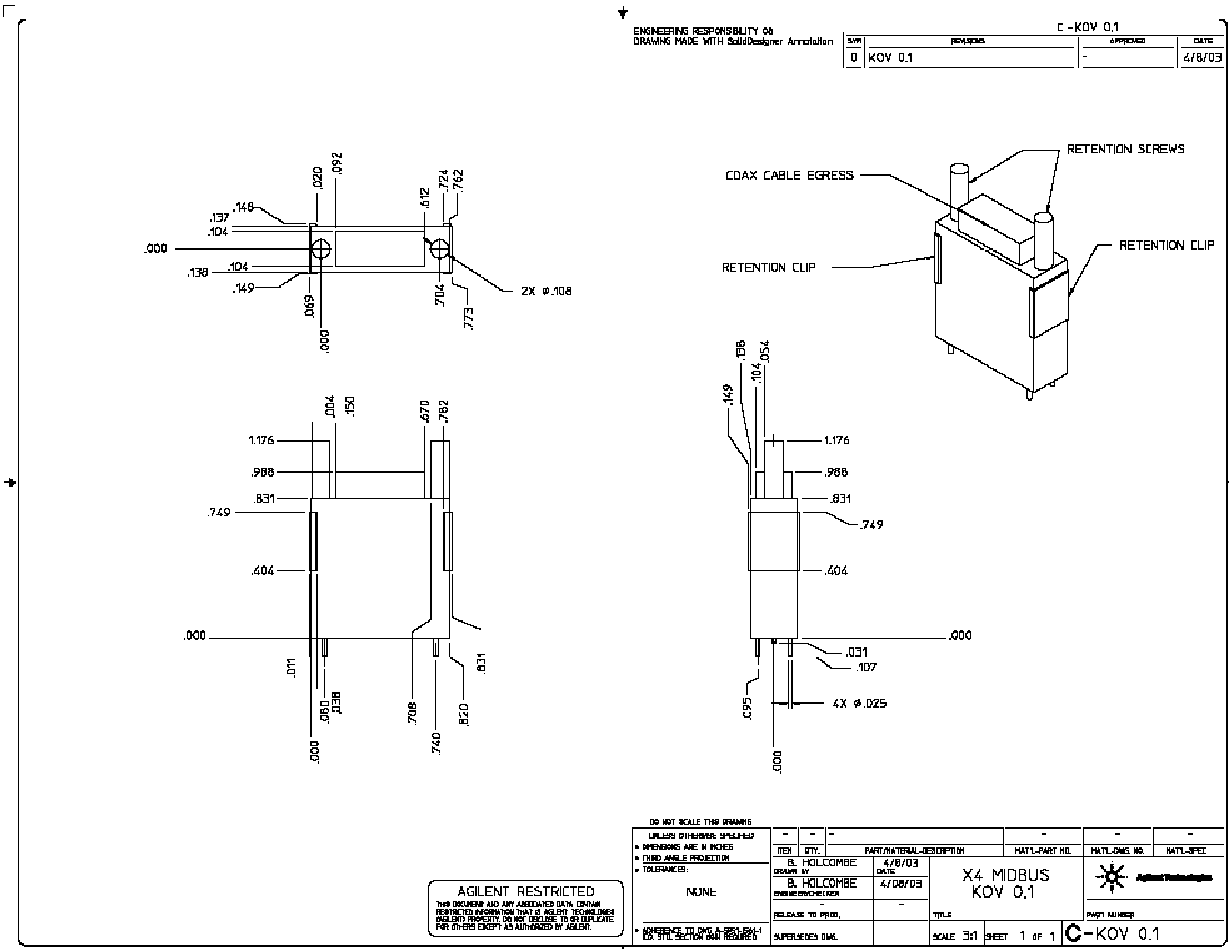


Figure 2- PCI Express™ LAI Keepout Volume

3.1.4 N4228A – ½ Size midbus Keepout Volume



3.2 Reference Clock

3.2.1 Reference Clock Header

A 3-pin header (1 by 3, 0.05" center spacing) will provide the connection for reference clock to the LAI. A small high impedance clock probe from the LAI will connect to this header and carry the REFCLKp and REFCLKn signals to the LAI. Note that an individual reference clock header is required for each PCI Express™ clock domain on the system.

The following are recommended part numbers for through-hole and surface mount versions of the 3-pin header for reference clock:

- Through-hole: Samtec* TMS-103-02-S-S
- Surface mount: Samtec* FTR-103-02-S-S

Table 1- Reference Clock header pinout

Signal	Pin Number
REFCLKp	1 (or 3) [1]
GND or N/C	2
REFCLKn	3 (or 1) [1]

Note: The LAI is not sensitive to the polarity of the reference clock. Therefore, the probe can be plugged onto the pin header in either orientation.

3.2.2 LAI Reference Clock Probe Keepout Volume

Keepout volumes for the reference clock probes are given in Figure 3.. The pin headers reside symmetrically within the keepout volume on the target system. For more specific information on keepout volumes for particular solutions please contact Agilent Technologies.

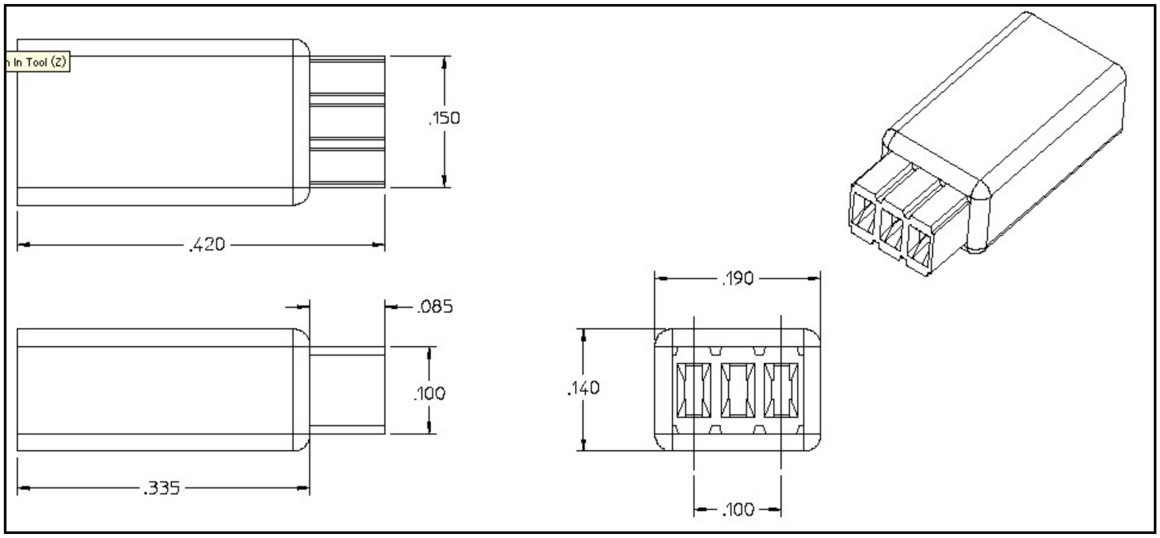


Figure 3- PCI Express™ Reference Clock Probe Keepout Volume

4 Electrical Design

This section contains electrical design details of the midbus LAI and the reference clock pin header. These details include LAI eye requirement definition, system impact due to LAI probe presence, LAI routing suggestions, load models, and pin assignments.

4.1 Midbus LAI

Logical probing of the PCI Express™ bus is achieved through tapping a small amount of energy off the probed signals and channeling this energy to the logic analyzer. In order to avoid excessive loading conditions, the use of tip resistors, or isolation resistors, is employed. These relatively high impedance tip resistors enable the logic analyzer to sample bus traffic without significantly loading the probed signals. A high-level block diagram of a generic PCI Express™ bus with a logic analyzer interface is given in Figure 4. Note that this would be repeated for each differential pair within a PCI Express™ link.

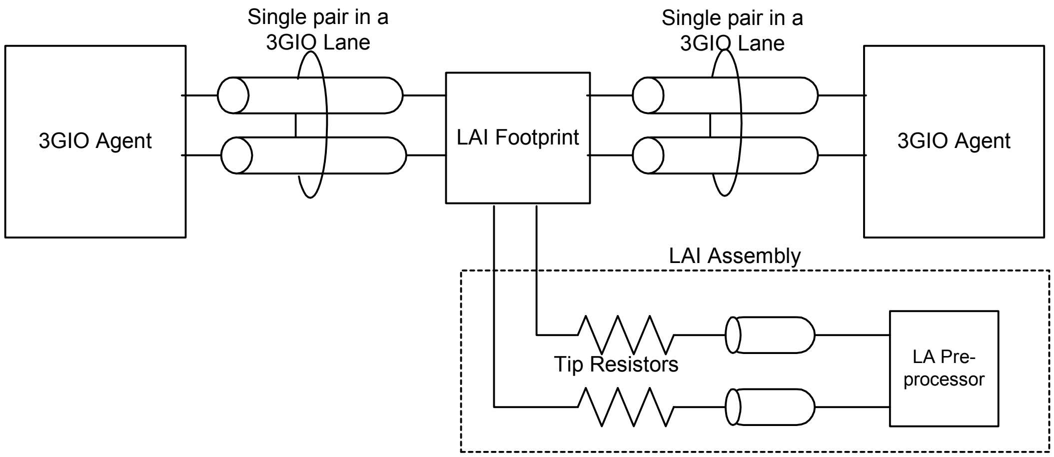


Figure 4- Block diagram example of a generic PCI Express™ bus with a LAI

4.1.1 LAI Placement within System Topology

In order for the LA to reliably capture logical transactions on the bus, adequate signal eye must be made available to the LAI. It is incumbent upon the platform designers to ensure that sufficient signal eye is available to the LAI while the LAI load is in place so that proper signal tracing is enabled. This must be verified via electrical simulation utilizing the load model provided in Figure 7.

The eye requirements are measured by eye height and eye width, forming a diamond shape. These requirements are described pictorially in Figure 5.

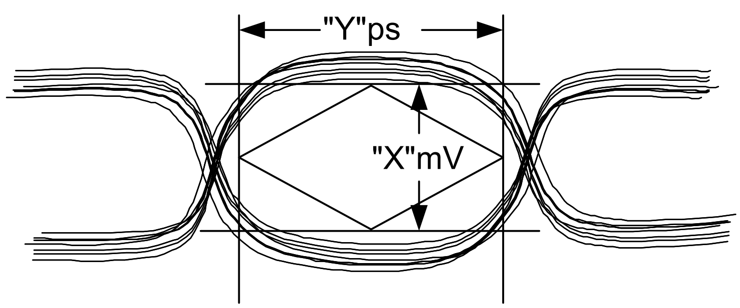


Figure 5- Example of eye specifications as seen at the LAI pad

Table 2 details the specific eye requirements for Agilent Technologies. Address questions to Agilent Technologies for the most current eye requirements.

Table 2- PCI Express™ LAI Footprint Placement Interconnect Specification-

	Agilent Technologies Specification
Min Eye height at LAI pad[1]	175mV
Min Eye Width at LAI pad	TBD
Length Matching Requirements-Differential Pairs[2]	+/-5mil
Length Matching Requirements-Pair to Pair	none

Note:

1- Measured in differential units, e.g. Vdiff = |2*(Vp - Vn)|

2- Interconnect must length match +/-5 mils from source to LAI footprint pad for each polarity of the differential pair.

The eye characteristics given in Table 2 must be maintained for all probed links, regardless of direction. Overall, these LAI placement specifications limit the electrical distance between the driver pin and the LAI attach point. Conceivably, probing both directions in lanes of a long PCI Express™ link may require two separate footprints and LAI assemblies, while probing both directions of relatively short links may be accomplished with one LAI. Regardless of implementation, refer to usage restrictions as listed in section 2- Overview and Configuration Support. The same LAI eye requirements exist for all links substrates (e.g. FR4, cables, etc.)

An additional constraint on LAI footprint placement involves the relative location of the AC coupling capacitors. The capacitors may be placed either between the driver and LAI, or between the LAI and receiver, as long as both capacitors of a differential pair are placed in the same fashion. Other pairs within a link do not need to maintain this capacitor placement configuration.

4.1.2 Impact on PCI Express™ Channel due to Probe Presence

Agilent will provide detailed information on impact as soon as detailed, measured information is available.

4.1.3 Routing Considerations Near/Through PCI Express™ LAI Footprint

Agilent will provide detailed information on Routing and Design Considerations at a later date.

4.1.3.1 Surface Layer Routing (on same side as LAI)

Figure 6 presents suggested routing for footprint negotiation in the case of surface (microstrip) routing when this routing is on the same side of board as LAI.

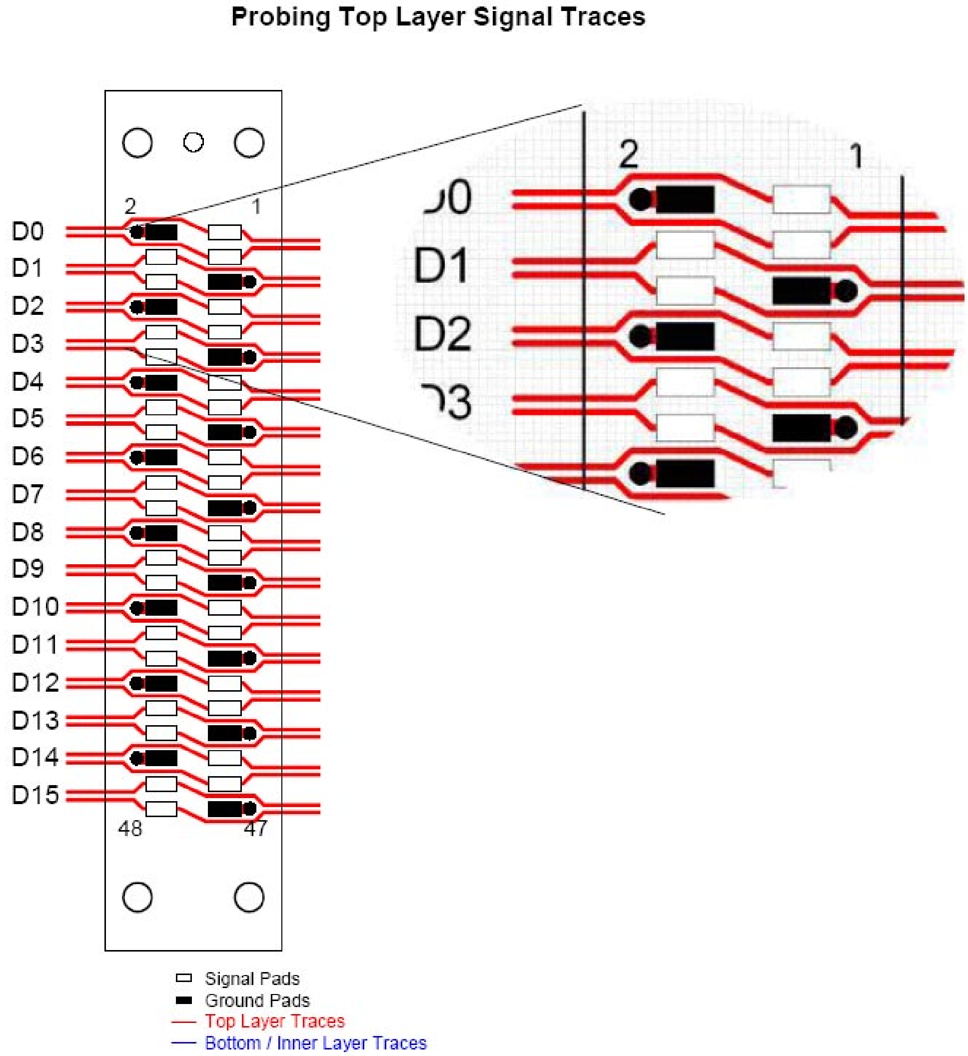
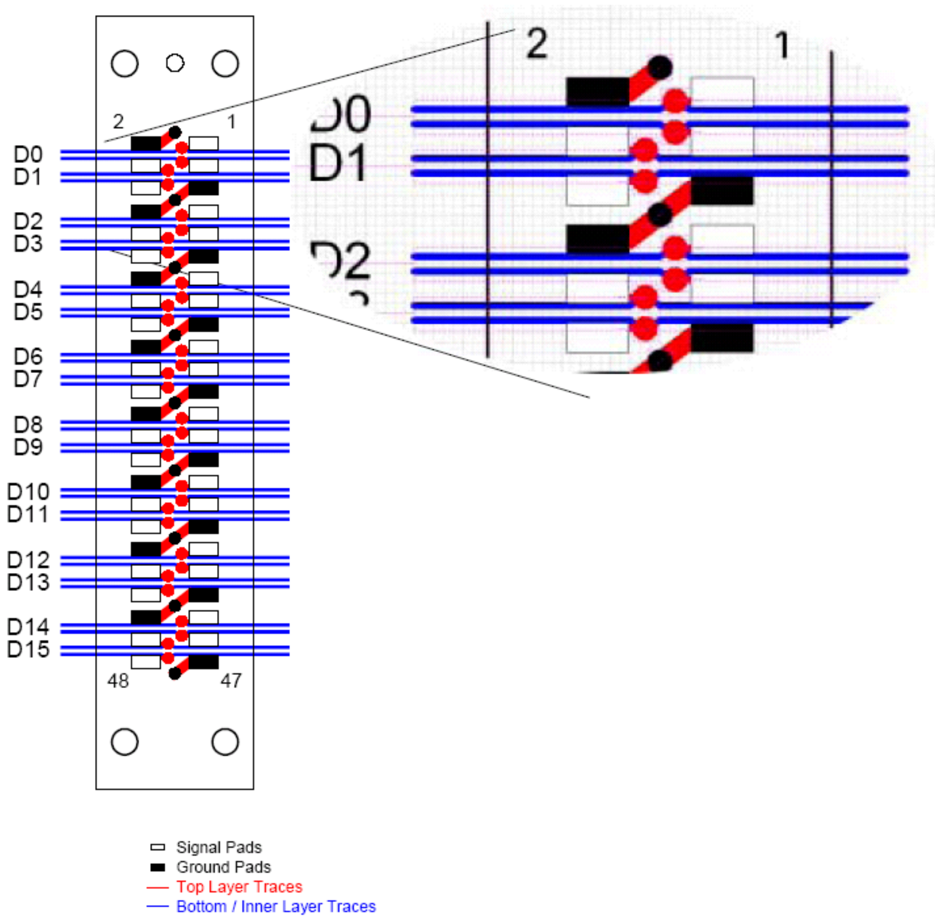


Figure 6- Suggested routing for microstrip traces on same layer as LAI

4.1.3.2 Inner layer and secondary side routing (surface layer opposite of LAI)

Probing Inner Layer Signal Traces



4.1.4 Load Models

4.1.4.1 Agilent Technologies* Load Model

The Agilent Technologies load model for the midbus LAI is given in Figure 7. This model is subject to change. For the most current models, it is recommended that the platform designer contact Agilent Technologies directly.

3GIO (PCI-Express) MidBus Probe Load Model
Using VNA Measured Data from 08-Jul-2002
Rev A3: 20 July 2002

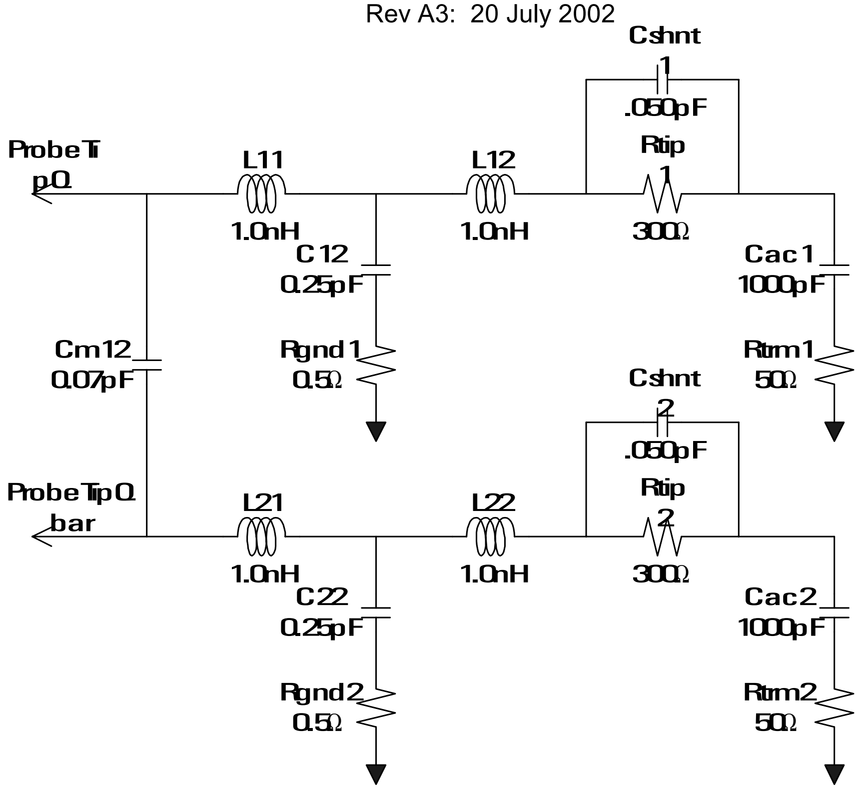


Figure 7- Load model for LAI

4.1.4.2 Load Model without LAI Installed

The model of the parasitic load on the system due to the LAI midbus footprint only (i.e. no LAI installed) is represented simply by a 0.2pF capacitor to ground. Note that if vias are associated with tapping the link for the LAI, those via parasitics would also need to be considered here in addition to the 0.2pF pad load.

4.1.5 PCI Express™ LAI Pin Assignments

There is flexibility in the arrangement and layout of the midbus footprint. Agilent will provide configuration of the LAI to support the following midbus layouts. There is a detailed view of these connections below. Appendix B also contains a high level depiction of the same midbus footprint.

The pinout for the PCI Express™ LAI is given in – Full Size Midbus Pin Assignment

Table 3. It is imperative that designers understand there is some freedom associated with the pin/signal assignment relationship. These notes are given here:

Footprint Channel vs. Lane/Link Designations

- Channel= either an upstream OR downstream differential pair for a given lane
- C<letter>= the designator for a Channel which accepts a given differential pair of signals
- C<letter><p or n>= the two signals of the differential pair. The signals within a given pair may be assigned to either x or y regardless of polarity

General Rules for Signal Pair Assignment

The differential pairs that make up the PCI Express™ links must be assigned to specific pins of the footprint. However, there is some freedom in this pair assignment in order to minimize routing constraints on the platform. Additionally, note that the channel to footprint assignment configuration is closely related to the "direction" of the probed link . More specifically, a bi-directional pin assignment is different from a unidirectional pin assignment. See the following tables contained in this section for more information.

4.1.5.1 – Full Size Midbus Pin Assignment

Table 3- General PCI Express™ LAI Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND
26	GND	25	CIp
28	CJp	27	CIn
30	CJn	29	GND
32	GND	31	CKp
34	CLp	33	CKn
36	CLn	35	GND
38	GND	37	CMp
40	CNp	39	CMn
42	CNn	41	GND
44	GND	43	CPp
46	CQp	45	CPn
48	CQn	47	GND

Table 4- x16 (Standard) PCI Express™ LAI Pinout[1, 2, 3]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p
4	C1p	3	C0n
6	C1n	5	GND
8	GND	7	C2p
10	C3p	9	C2n
12	C3n	11	GND
14	GND	13	C4p
16	C5p	15	C4n
18	C5n	17	GND
20	GND	19	C6p
22	C7p	21	C6n
24	C7n	23	GND
26	GND	25	C8p
28	C9p	27	C8n
30	C9n	29	GND
32	GND	31	C10p
34	C11p	33	C10n
36	C11n	35	GND
38	GND	37	C12p
40	C13p	39	C12n
42	C13n	41	GND
44	GND	43	C14p
46	C15p	45	C14n
48	C15n	47	GND

Notes:

1. Polarity (p and n) of each differential pair may be swapped
2. This configuration can only probe either upstream 16 channels OR 16 downstream channels with one LAI Please see Table 7 for a configuration that supports interleaved x16 traffic amongst two LAI Footprints.
3. Entire link assignment may be reversed in LAI. For example, channel 0 may be swapped in above table with channel 15, channel 1 with channel 14, etc. If swapping upstream, must also swap downstream (and vice versa).

Table 5- x16 (Split) specific PCI Express™ LAI Pinout[1, 2, 3, 4]

Midbus Connector 1				Midbus Connector 2			
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C8p- Upstream	2	GND	1	C0p- Upstream
4	C8p- Downstream	3	C8n- Upstream	4	C0p- Downstream	3	C0n- Upstream
6	C8n- Downstream	5	GND	6	C0n- Downstream	5	GND
8	GND	7	C9p- Upstream	8	GND	7	C1p- Upstream
10	C9p- Downstream	9	C9n- Upstream	10	C1p- Downstream	9	C1n- Upstream
12	C9n- Downstream	11	GND	12	C1n- Downstream	11	GND
14	GND	13	C10p- Upstream	14	GND	13	C2p- Upstream
16	C10p- Downstream	15	C10n- Upstream	16	C2p- Downstream	15	C2n- Upstream
18	C10n- Downstream	17	GND	18	C2n- Downstream	17	GND
20	GND	19	C11p- Upstream	20	GND	19	C3p- Upstream
22	C11p- Downstream	21	C11n- Upstream	22	C3p- Downstream	21	C3n- Upstream
24	C11n- Downstream	23	GND	24	C3n- Downstream	23	GND
26	GND	25	C12p- Upstream	26	GND	25	C4p- Upstream
28	C12p- Downstream	27	C12n- Upstream	28	C4p- Downstream	27	C4n- Upstream
30	C12n- Downstream	29	GND	30	C4n- Downstream	29	GND
32	GND	31	C13p- Upstream	32	GND	31	C5p- Upstream
34	C13p- Downstream	33	C13n- Upstream	34	C5p- Downstream	33	C5n- Upstream
36	C13n- Downstream	35	GND	36	C5n- Downstream	35	GND
38	GND	37	C14p- Upstream	38	GND	37	C6p- Upstream
40	C14p- Downstream	39	C14n- Upstream	40	C6p- Downstream	39	C6n- Upstream
42	C14n- Downstream	41	GND	42	C6n- Downstream	41	GND
44	GND	43	C15p- Upstream	44	GND	43	C7p- Upstream
46	C15p- Downstream	45	C15n- Upstream	46	C7p- Downstream	45	C7n- Upstream
48	C15n- Downstream	47	GND	48	C7n- Downstream	47	GND

Notes:

1. Polarity (p and n) of each differential pair may be swapped
2. Entire link assignment may be reversed in LAI. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).
3. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped

Table 8- x8 (Bi-directional) specific PCI Express™ LAI Pinout[1, 2, 3, 4]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND
26	GND	25	C4p- Upstream
28	C4p- Downstream	27	C4n- Upstream
30	C4n- Downstream	29	GND
32	GND	31	C5p- Upstream
34	C5p- Downstream	33	C5n- Upstream
36	C5n- Downstream	35	GND
38	GND	37	C6p- Upstream
40	C6p- Downstream	39	C6n- Upstream
42	C6n- Downstream	41	GND
44	GND	43	C7p- Upstream
46	C7p- Downstream	45	C7n- Upstream
48	C7n- Downstream	47	GND

Notes:

1. Polarity (p and n) of each differential pair may be swapped
2. Can probe upstream 8 channels AND downstream 8 channels with one LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-upstream may be swapped in above table with channel 7-upstream, channel 1-upstream with channel 6-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).
4. Upstream and downstream pin assignments may be swapped. For example, channel0-upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped

Table 9- Dual x4 (Bi-directional) specific PCI Express™ LAI Pinout[1, 2, 3, 4 ,5]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	C2p- Upstream1
16	C2p- Downstream1	15	C2n- Upstream1
18	C2n- Downstream1	17	GND
20	GND	19	C3p- Upstream1
22	C3p- Downstream1	21	C3n- Upstream1
24	C3n- Downstream1	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	C2p- Upstream2
40	C2p- Downstream2	39	C2n- Upstream2
42	C2n- Downstream2	41	GND
44	GND	43	C3p- Upstream2
46	C3p- Downstream2	45	C3n- Upstream2
48	C3n- Downstream2	47	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe upstream 4 channels AND downstream 4 channels of TWO x4 links with one LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-upstream1 may be swapped in above table with channel 3-upstream, channel 1-upstream with channel 2-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).
4. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped
5. Single Link Configuration also supported.

Table 10- Dual x2 (Bi-directional) specific PCI Express™ LAI Pinout[1, 2, 3, 4, 5]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	C1p- Upstream2
34	C1p- Downstream2	33	C1n- Upstream2
36	C1n- Downstream2	35	GND
38	GND	37	nc
40	nc	39	nc
42	nc	41	GND
44	GND	43	nc
46	nc	45	nc
48	nc	47	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe upstream 2 channels AND downstream 2 channels of two x2 links with one LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-upstream1 may be swapped in above table with channel 1-upstream, etc. If swapping upstream, must also swap downstream (and vice versa).
4. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped
5. Single Link Configuration also supported.

Table 11- Dual x1 (Bi-directional) specific PCI Express™ LAI Pinout[1, 2, 3, 4]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND
26	GND	25	C0p- Upstream2
28	C0p- Downstream2	27	C0n- Upstream2
30	C0n- Downstream2	29	GND
32	GND	31	nc
34	nc	33	nc
36	Nc	35	GND
38	GND	37	nc
40	Nc	39	nc
42	nc	41	GND
44	GND	43	nc
46	nc	45	nc
48	Nc	47	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe upstream 1 channel AND 1 downstream channel of two x1 links with one LAI
3. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream
4. Single Link Configuration also supported.

4.1.5.2 – Half Size Midbus Pin Assignment

Table 12 - General 8 Channel PCI Express* Pinout

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	CAp
4	CBp	3	CAn
6	CBn	5	GND
8	GND	7	CCp
10	CDp	9	CCn
12	CDn	11	GND
14	GND	13	CEp
16	CFp	15	CEn
18	CFn	17	GND
20	GND	19	CGp
22	CHp	21	CGn
24	CHn	23	GND

Table 13 - x8 (unidirectional) specific 8-Channel PCI Express* LAI Pinout[1,2,3]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- DirectionA
4	C1p- DirectionA	3	C0n- DirectionA
6	C1n- DirectionA	5	GND
8	GND	7	C2p- DirectionA
10	C3p- DirectionA	9	C2n- DirectionA
12	C3n- DirectionA	11	GND
14	GND	13	C4p- DirectionA
16	C5p- DirectionA	15	C4n- DirectionA
18	C5n- DirectionA	17	GND
20	GND	19	C6p- DirectionA
22	C7p- DirectionA	21	C6n- DirectionA
24	C7n- DirectionA	23	GND

Notes:

1. Polarity (p and n) of each differential pair may be swapped
2. Can probe DirectionA 8 channels with one 8-channel LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-DirectionA may be swapped in above table with channel 7-DirectionA, channel 1-DirectionA with channel 6-DirectionA, etc.

Table 14- x4 (Bi-directional) specific 8 Channel PCI Express* LAI Pinout[1,2,3,4]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream
4	C0p- Downstream	3	C0n- Upstream
6	C0n- Downstream	5	GND
8	GND	7	C1p- Upstream
10	C1p- Downstream	9	C1n- Upstream
12	C1n- Downstream	11	GND
14	GND	13	C2p- Upstream
16	C2p- Downstream	15	C2n- Upstream
18	C2n- Downstream	17	GND
20	GND	19	C3p- Upstream
22	C3p- Downstream	21	C3n- Upstream
24	C3n- Downstream	23	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe Upstream 4 channels AND Downstream 4 channels of ONE x4 link with one 8 channel LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-upstream may be swapped in above table with channel 3-upstream, channel 1-upstream with channel 2-upstream, etc.
4. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped

Table 15 - x4 (2 unidirectional) specific 8 Channel PCI Express* LAI Pinout[1,2,3]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- DirectionA
4	C0p- DirectionB	3	C0n- DirectionA
6	C0n- DirectionB	5	GND
8	GND	7	C1p- DirectionA
10	C1p- DirectionB	9	C1n- DirectionA
12	C1n- DirectionB	11	GND
14	GND	13	C2p- DirectionA
16	C2p- DirectionB	15	C2n- DirectionA
18	C2n- DirectionB	17	GND
20	GND	19	C3p- DirectionA
22	C3p- DirectionB	21	C3n- DirectionA
24	C3n- DirectionB	23	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe DirectionA 4 channels and DirectionB 4 channels with one 8 channel LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-DirectionA may be swapped in above table with channel 3- DirectionA, channel 1- DirectionA with channel 2- DirectionA, etc.

Table 16- x2 (Bi-directional) specific 8 Channel PCI Express* LAI Pinout[1,2,3,4,5]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	C1p- Upstream1
10	C1p- Downstream1	9	C1n- Upstream1
12	C1n- Downstream1	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	C0p- Upstream1
16	C0p- Downstream1	15	C0n- Upstream1
18	C0n- Downstream1	17	GND
20	GND	19	C1p- Upstream1
22	C1p- Downstream1	21	C1n- Upstream1
24	C1n- Downstream1	23	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe upstream 2 channels AND downstream 2 channels of ONE x2 link with one 8 Channel LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-upstream1 may be swapped in above tables with channel 1-upstream1, etc.
4. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream, etc. Note that if one channel of upstream swapped with downstream, all channels upstream and downstream channels must be swapped
5. Consult your LA Vendor for capabilities of this configuration

Table 17- x2 (2 unidirectional) specific 8 Channel PCI Express* LAI Pinout[1,2,3,4]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- DirectionA
4	C0p- DirectionB	3	C0n- DirectionA
6	C0n- DirectionB	5	GND
8	GND	7	C1p- DirectionA
10	C1p- DirectionB	9	C1n- DirectionA
12	C1n- DirectionB	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	C0p- DirectionA
16	C0p- DirectionB	15	C0n- DirectionA
18	C0n- DirectionB	17	GND
20	GND	19	C1p- DirectionA
22	C1p- DirectionB	21	C1n- DirectionA
24	C1n- DirectionB	23	C0p- DirectionA

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe DirectionA 2 channels AND DirectionB 2 channels of ONE x2 link with one 8 Channel LAI
3. Entire link assignment may be reversed in LAI. For example, channel 0-DirectionA may be swapped in above tables with channel 1- DirectionA, etc
4. Consult your LA Vendor for capabilities of this configuration

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Table 18- x1 (Bi-directional) specific 8 Channel PCI Express* LAI Pinout[1,2,3]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- Upstream1
4	C0p- Downstream1	3	C0n- Upstream1
6	C0n- Downstream1	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	C0p- Upstream1
10	C0p- Downstream1	9	C0n- Upstream1
12	C0n- Downstream1	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	C0p- Upstream1
16	C0p- Downstream1	15	C0n- Upstream1
18	C0n- Downstream1	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	C0p- Upstream1
22	C0p- Downstream1	21	C0n- Upstream1
24	C0n- Downstream1	23	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe upstream channel AND downstream channel of ONE x1 link with one 8 Channel LAI
3. Upstream and downstream pin assignments may be swapped. For example, channel0- upstream may be swapped with channel 0- downstream

Table 19 - x1 (2 unidirectional) specific 8 Channel PCI Express* LAI Pinout[1,2]

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	C0p- DirectionA
4	C0p- DirectionB	3	C0n- DirectionA
6	C0n- DirectionB	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	C0p- DirectionA
10	C0p- DirectionB	9	C0n- DirectionA
12	C0n- DirectionB	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	C0p- DirectionA
16	C0p- DirectionB	15	C0n- DirectionA
18	C0n- DirectionB	17	GND
20	GND	19	nc
22	nc	21	nc
24	nc	23	GND

or

Pin #	Signal Name	Pin #	Signal Name
2	GND	1	nc
4	nc	3	nc
6	nc	5	GND
8	GND	7	nc
10	nc	9	nc
12	nc	11	GND
14	GND	13	nc
16	nc	15	nc
18	nc	17	GND
20	GND	19	C0p- DirectionA
22	C0p- DirectionB	21	C0n- DirectionA
24	C0n- DirectionB	23	GND

Notes:

1. Polarity (p and n) of the differential pair may be swapped
2. Can probe DirectionA 1 channel AND DirectionB 1 channel of ONE x1 link with one 8 Channel LA

4.2 Reference Clock

4.2.1 LAI Reference Clock Electrical Requirements

Table 20 - LAI electrical requirements on the differential reference clock signals

LAI Requirement	Symbol	Min	Max	Comments
Differential Voltage at Ref Clock Attach Point	Vdiff	0.8V	5V	Vdiff= |2*(Vrefclockp - Vrefclockn)|
Reference Clock Frequency (with SSC and/or frequency margining) [1]	f	90MHz	110MHz	

Note:

1. If reference clock tolerance is less than +/-150 PPM, there is no need for providing reference to the LAI. If the reference clock tolerance is greater than +/-150 PPM, there is a need for providing reference to the LAI.

4.2.2 LAI Reference Clock Probe Load Model

Load models for the reference clock probe are given in this section. System designers will be expected to perform simulations of the reference clock networks with the header and LAI load models to ensure good signal integrity of the reference clocks at the header to the LAI. The pin header parasitics may be obtained from the connector vendor.

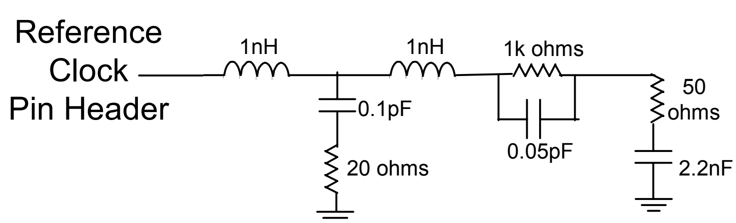

Figure 8- Agilent Technologies PCI Express™ Reference Clock Probe Load Model

5 Appendix A- PCI Express™ Probing Design Review Checklist

The following tables serve as a guide to review a platform (schematics and layout) with regard to PCI Express™ probing.

5.1 General Considerations

PASS	FAIL	NA	ISSUE
			Ideally, all PCI Express™ links in the system should be observable with LA tools either using “mid-bus” probing or through a add-in card interposer.
			If any PCI Express™ links are not observable with LA tools (see previous item) then the design and validation team(s) should agree that this is acceptable.

5.2 Mid-bus Probing Configurations

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint in the system, the number of links and sizes of those links within a footprint must meet the requirements of section 2.1 of the probing design guide. (For example, a single mid-bus footprint can contain the upstream channels of one x16 link or both the upstream and downstream channels of one x8 link.)
			If the configuration of the links within a mid-bus footprint does not meet the requirements of the previous item, then this configuration must be confirmed with Agilent.
			If a reference clock is required by the LAI then a connector for the reference clock must be provided for each PCI Express™ reference clock domain.
			Reference clock is required if spread spectrum clocking (SSC) is used and can’t be disabled in the system.
			Reference clock is required if testing with SSC is needed (because problem does not manifest with SSC disabled.)
			Reference clock is required if the link frequency is intentionally margin tested outside the standard +/-150ppm tolerance.

			Reference clock is required if the link reference operates outside the +/-300ppm tolerance imposed by the current LAI tools.
			For each reference clock provided to the LAI, is the clock properly terminated in the system?

5.3 Mechanical Considerations

5.3.1 Mid-bus Footprint(s)

PASS	FAIL	NA	ISSUE
			Verify that each mid-bus footprint matches the specifications in the probing design guide:
			▪ Pad size, spacing, arrangement.
			▪ Hole sizes, locations, tolerance, plating.
			▪ Solder mask requirements.
			▪ Pad plating requirements.
			▪ Pin numbering.
			▪ Component keepout requirements.
			Probe keepout requirements are met
			Verify that egress for probe cables is provided.

5.3.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Verify that each reference clock header matches the specifications in the probing design guide:
			▪ Verify footprint against the Samtec specification for either the SMT header (FTR-103-02-S-S) or the through-hole header (TMS-103-02-S-S). Check pad and hole size, spacing, arrangement, etc.
			▪ Verify pinout (pin 1 – REFCLKp, pin 2 – GND/NC , pin3 – REFCLKn or vise-versa)
			Reference clock probe keepout requirements are met.
			Verify that egress for reference clock probe cables is provided.

5.4 Electrical Considerations

5.4.1 Mid-bus Footprint(s):

PASS	FAIL	NA	ISSUE
			For each mid-bus footprint, have loss and jitter numbers at the LAI footprint pads been calculated and do they meet the requirements for the LAI tools?
			Have the constraints on AC coupling capacitor location for probing been met? (Each pair of capacitors may be placed on either side of the LAI footprint for each differential signal pair, but the location relationship can be varied for different differential pairs in the link.)
			For each link probed, system simulations must be performed with LAI load models included in order to verify that the system will work with LAI attached. Verify that the loss and jitter at the system receivers is within spec when the LAI load is installed.
			For each link probed using a mid-bus footprint, system simulations must be performed with the footprint model included in order to verify that the system will work with the footprint *without* the LAI attached
			Does system layout follow the guidelines on via and trace characteristics in the probing design guide?
			Does system layout follow the routing guidelines in the probing design guide? Are the differential pairs routed appropriately? (matched length, identical paths/vias, etc.)
			Verify pin assignment of the mid-bus footprint against the specifications in the probing design guide:
			▪ All channels of a single direction of a link must connect to the same footprint.
			▪ It is preferable (but not required) that both directions of a link connect to the same footprint.
			▪ All unused pads on the LAI may be left unconnected.
			▪ Verify specific pinouts against tables in the probing design guide.

5.4.2 Reference Clock Header(s)

PASS	FAIL	NA	ISSUE
			Are LAI reference clock electrical requirements met?
			▪ Differential voltage
			▪ Absolute voltage
			▪ Frequency
			Simulations of the reference clock network(s) must be performed using load models for the LAI reference clock probe to ensure good signal integrity to the LAI:
			▪ Sims with load model look good?

6 Appendix B- High Level View of Supported Midbus footprint configurations

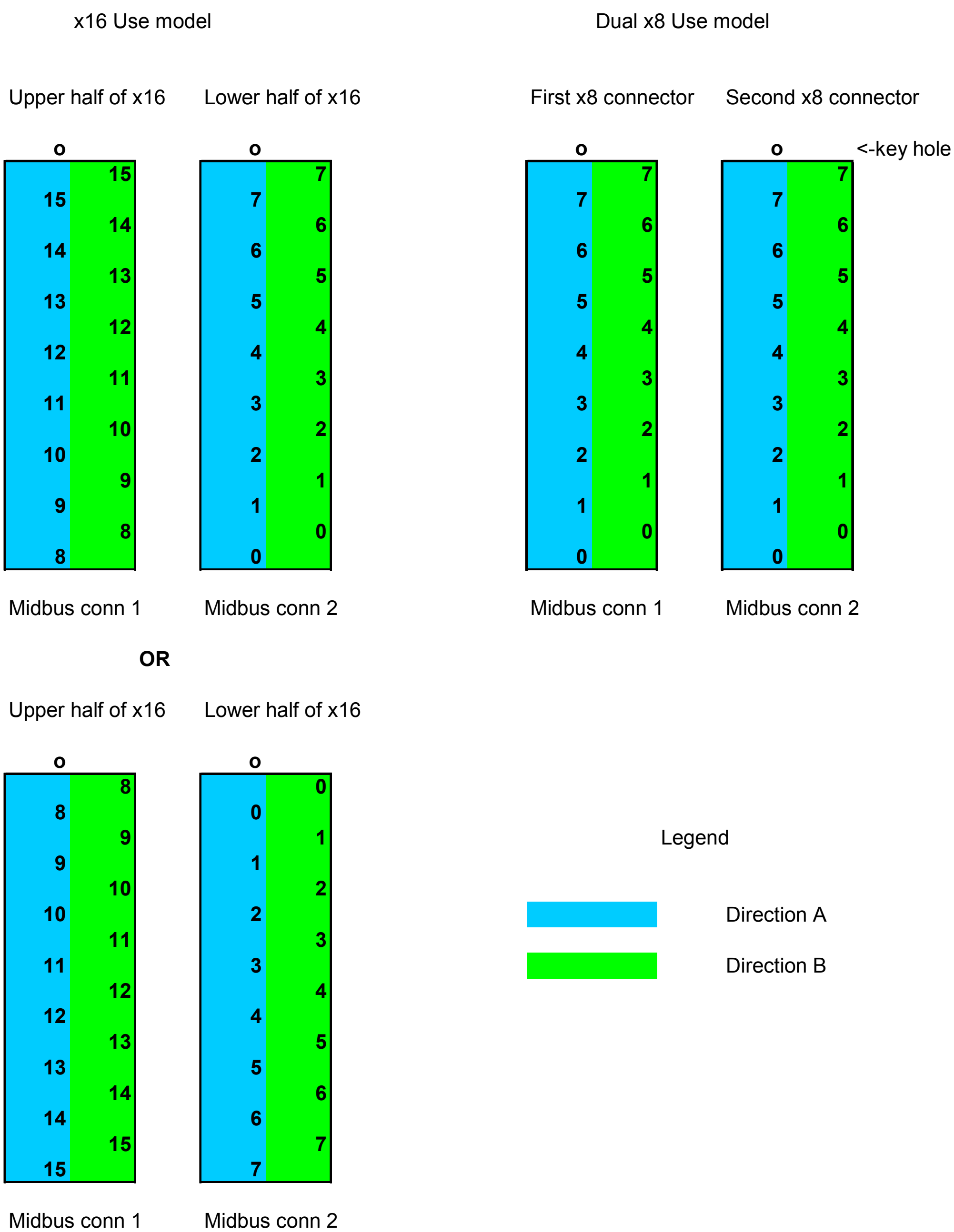

Figure 9 - High Level View of x16 Midbus Configuration Options

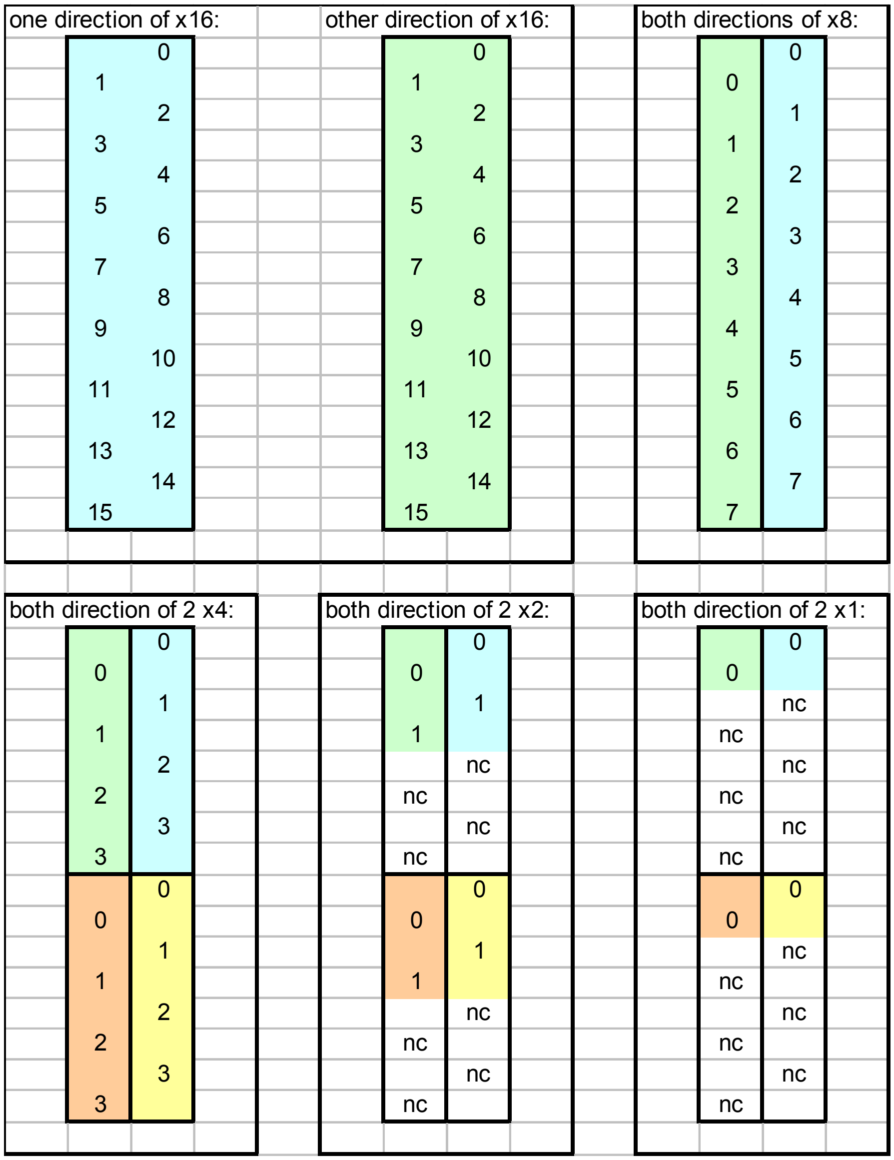

Figure 10 - High Level View of x8 Midbus Configuration Options